AMENDMENTS TO THE CLAIMS

Claim 1. (Currently amended): An integrated input/output controller integrated into a single integrated circuit device, comprising:

a host interface subsystem coupled to [[a]] at least one host for receiving ~~to receive~~ host commands and to transceive data blocks with the at least one host in response to the host commands, said host interface system including a command decode controller for parsing host commands to identify data flow type host commands and non data flow type commands; ~~and~~

a mapping controller coupled to the host interface subsystem for mapping logical block addresses of the data flow type host commands into peripheral block addresses of one or more peripherals; ~~to transceive the data blocks with the one or more peripherals~~ and

a peripheral interface subsystem coupled to one or more peripherals for transceiving data blocks with the one or more peripherals using the peripheral block addresses generated by the mapping controller;

wherein

for each data flow type host command, said command decode controller communicates an associated logical block address to the mapping controller, said mapping controller converts the associated logical block address to an associated peripheral block address, and said peripheral interface subsystem accesses the one or more peripherals using said associated peripheral block address.

Claim 2. (Canceled)

Claim 3. (Withdrawn) The integrated input/output (I/O) controller of claim 1, wherein: ~~including circuits to perform:~~

said host commands are ~~receiving a~~ high level I/O commands received from a host;

said command decode controller includes circuits for parsing the high level I/O commands to determine whether to read or write data;

said mapping controller includes circuits for mapping the high level I/O request into one or more peripheral I/O commands, the one or more peripheral I/O commands indicating which of the one or more peripherals and which respective data locations are to be accessed; and

said peripheral interface subsystem includes circuits for servicing the high level I/O request by reading or writing data between the host and the one or more peripherals using the respective data locations.

Claim 4. (Withdrawn) The integrated I/O controller of claim 3, further including circuits to perform: prior to servicing the high level I/O request, storing data temporarily into an external cache buffer from the data flow between the host and the one or more peripherals.

Claim 5. (Withdrawn) The integrated I/O controller of claim 3, wherein [[,]] each of the one or more peripheral I/O commands further indicates the number of blocks of data to be serviced.

Claim 6. (Withdrawn) The integrated I/O controller of claim 3, wherein said mapping controller ~~mapping the high level I/O request into one or more peripheral I/O commands~~ includes circuits to perform:

parsing a high level command from an I/O request packet,

decoding the high level command and generating a range operation request in response thereto, and

generating the one or more peripheral I/O commands in response to the range operation request.

Claim 7. (Withdrawn) The integrated I/O controller of claim 3, wherein [[,]] each of the one or more peripherals are storage disks and each of the one or more peripheral I/O commands are Small Computer System Interface (SCSI) disk I/O commands.

Claim 8. (Withdrawn) The integrated I/O controller of claim 3, wherein [[,]] the high level I/O command is a command of a Small Computer System Interface (SCSI) Command Descriptor Block (CDB) standard.

Claim 9. (Withdrawn) The integrated I/O controller of claim 3, wherein [[,]] the circuits of the integrated I/O controller are hard wired circuits.

Claim 10. (Withdrawn) The integrated I/O controller of claim 3, wherein [[,]] the circuits of the integrated I/O controller are microcoded circuits and state machines operating concurrently.

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Claim 11. (Withdrawn) The integrated I/O controller of claim 3, wherein [[,]] the circuits of the integrated I/O controller are hard wired circuits, microcoded circuits and state machines operating concurrently.

Claim 12. (Withdrawn) The integrated I/O controller of claim 3, wherein [[,]] the circuits of the integrated I/O controller are programmable micro-controllers operating concurrently.

Claim 13. (Canceled)

Claim 14. (Withdrawn) The integrated input/output controller of claim 1, further comprising [[:]] a micro-controller subsystem coupled to the host interface subsystem for processing non data flow type host commands ~~and the peripheral interface subsystem, the micro-controller subsystem to perform initialization and to process errors and exception events~~.

Claim 15. (Withdrawn) The integrated input/output controller of claim 1, ~~13~~ further comprising:

a cache manager coupled to the host interface subsystem and the peripheral interface subsystem, the cache manager to manage entries in a cache buffer to temporarily store data of the data flow between the peripheral and the host.

Claim 16. (Withdrawn) The integrated input/output controller of claim 15, further comprising:

a buffer manager coupled to the host interface subsystem, the peripheral interface subsystem, and the cache manager, the buffer manager to manage data storage in the cache buffer.

Claim 17. (Withdrawn) The integrated input/output controller of claim 1, wherein [[,]] the host interface subsystem includes a fibre channel host port to transceive data with the host using a fibre channel protocol.

Claim 18. (Withdrawn) The integrated input/output controller of claim 1, wherein [[,]] the host interface subsystem includes a host exchange controller to control the physical connection and protocol of the host.

Claim 19. (Canceled)

Claim 20. (Withdrawn) The integrated input/output controller of claim 1, wherein [[,]] the peripheral interface subsystem includes a peripheral exchange controller to control the physical connection and protocol of the peripheral.

Claim 21. (Withdrawn) The integrated input/output controller of claim 1, wherein [[,]] the peripheral interface subsystem includes a Fibrechannel disk port to transceive data with the peripheral using a Fibrechannel protocol.

Claims 22-27. (Canceled)

Claim 28. (Withdrawn) The integrated input/output controller of claim 1, further comprising:

a micro-controller coupled to the host interface subsystem, the micro-controller to perform initialization and handle error and exception handling events.

Claim 29. (Withdrawn) The integrated input/output controller of claim 28, wherein [[,]] the host interface subsystem includes a fibre channel host port to transceive data with the <u>at least one host</u> ~~one or more servers~~ using a fibre channel protocol.

Claim 30. (Canceled)

Claim 31. (Withdrawn) The integrated input/output controller of claim 1, ~~30~~ wherein [[,]] the command decode controller ~~to~~ further validates a host command and ~~to~~ initiates execution of the host command by the integrated input/output controller.

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Claim 32. (Withdrawn) The integrated input/output controller of claim 1, ~~30~~ wherein [[,]] the command decode controller maintains a ~~to further validate a host command and to queue the host command in a queue to be executed in an order, the~~ command queue for each ~~associated with a~~ volume accessible by the at least one host ~~one of the one or more a servers~~ to further validate a host command and to queue the host command for execution.

Claim 33. (Withdrawn) The integrated input/output controller of claim 1, ~~30~~ wherein [[,]] the command decode controller ~~to~~ further validates a host command and, if ~~to determines that~~ the host command is determined to be invalid, the host command is passed to a ~~the~~ micro-controller subsystem ~~to process the invalidity~~ for processing as a non data flow command.

Claim 34. (Withdrawn) The integrated input/output controller of claim 1, ~~30~~ wherein [[,]] the host commands ~~packets~~ are high level input/output requests.

Claim 35. (Canceled)

Claim 36. (Withdrawn) The integrated input/output controller of claim 28, wherein [[,]] the integrated input/output controller is an integrated RAID controller to transceive data between one or more disks of at least one disk array and the integrated input/output controller further comprises:

a disk interface to couple to the one or more disks of the at least one disk array to transceive the data to or from the at least one host; ~~one or more servers;~~ and

the mapping controller is a RAID mapping controller to flexibly control the mapping of blocks of data storage on the one or more disks of the at least one disk array.

Claim 37. (Withdrawn) The integrated input/output controller of claim 36, wherein [[,]] the one or more disks of the at least one array of disks are magnetic storage media, optical storage media or semiconductor storage media.

Claim 38. (Withdrawn) The integrated input/output controller of claim 36, wherein [[,]] the disk interface subsystem includes one or more fibre channel disk ports to transceive data with the one or more disks of the at least one disk array using a fibre channel protocol.

Claim 39. (Withdrawn) The integrated input/output controller of claim 28, wherein [[,]] the mapping controller provides RAID mapping automation.

Claim 40. (Withdrawn) The integrated input/output controller of claim 28, wherein [[,]] the mapping controller is programmable hardware to flexibly control the mapping of blocks of data storage on the one or more disks of the at least one disk array.

Claim 41. (Withdrawn) The integrated input/output controller of claim 28, wherein [[,]] the mapping controller ~~to~~ receives a requested command input packet to generate expanded command output packets in response thereto, the requested command input packet functions as a logical address and the expanded command output packets function as physical addresses.

Claim 42. (Withdrawn) The integrated input/output controller of claim 28, further comprising:

a buffer manager and a cache manager, the buffer manager and the cache manager being coupled ~~to couple~~ to a cache buffer and a cache table buffer respectively to flexibly control the reading and writing of data to and from the mapped data storage on the one or more disks of the at least one disk array.

Claim 43. (Withdrawn) The integrated input/output controller of claim 1, ~~2~~ wherein said integrated input/output controller is a ~~comprising~~ part of a storage area network, and the storage area network comprises: ~~comprising:~~

at least one server to couple to a network;

at least one disk array having a plurality of disks; and

at least one ~~fibre channel~~ controller to couple to at least one server and at least one disk array, wherein the at least one ~~fibre channel~~ controller reads and writes ~~to read and write~~ data between the at least one server and the at least one disk array, the at least one ~~fiber channel~~ controller having

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a cache memory,

a microprocessor to initialize the ~~fiber channel~~ controller upon power up and reset, and

a programmable random access memory (PRAM) to store initialization instructions in firmware,

wherein the integrated input/output controller is connected to the storage area network and comprises a hardware redundant array of independent disks (RAID) controller to control the reading and writing of data between the at least one server and the at least one disk array.

Claim 44. (Withdrawn) The integrated input/output controller of claim 43, wherein the host interface subsystem receives data from the at least one server for storage into the one or more disks of the at least one disk array and transmits data to the at least one server for data accessed from the one or more disks of the at least one disk array;

the peripheral interface subsystem comprises a disk interface subsystem to couple to the one or more disks of the at least one disk array to transmit data to the one or more disks of the at least one disk array for storage and to receive data from the one or more disks of the at least one disk array when accessed, and

the mapping controller comprises a RAID mapping subsystem ~~to~~ flexibly controls the mapping of blocks of storage on the one or more disks of the at least one disk array.[[,]] ~~and~~

~~further comprising a micro-controller coupled to the host interface subsystem, the disk interface subsystem, and the RAID mapping subsystem for handling non-data flow commands, error and exception handling events as well as system initialization.~~

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Claim 45. (Withdrawn) The integrated input/output controller ~~storage area network~~ of claim 43 ~~for central data storage and management~~, wherein[[,]] the cache memory provides a cache data buffer and a cache table buffer for the integrated RAID controller integrated circuit.

Claim 46. (Withdrawn) The integrated input/output controller ~~storage area network~~ of claim 43 ~~for central data storage and management~~, wherein[[,]] the plurality of disks of the at least one array of disks are magnetic storage media, optical storage media or semiconductor storage media.

Claim 47. (Withdrawn) The integrated input/output (I/O) controller of claim 1, further comprising:

a mapping engine to map high level host I/O requests into low level I/O commands; and

a low level command manager to manage data read and data write accesses into and out of a peripheral device in response to the low level I/O commands.

Claim 48. (Withdrawn) The integrated input/output (I/O) controller of claim 47, further comprising:

a buffer manager to arbitrate access by the one or more servers and to control data reads and data writes into and out of a buffer memory.

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Claim 49. (Withdrawn) The integrated input/output (I/O) controller of claim 47, further comprising a micro-controller to handle non-data flow commands, system initialization and error handling exception conditions.

Claim 50. (Withdrawn) The integrated input/output (I/O) controller of claim 47, wherein the integrated I/O controller is a RAID controller and the peripheral device is a plurality of disks responsive to disk I/O commands.

Claims 51-52. (Canceled)

Claim 53 (New) The controller of claim 1, wherein data flow host commands comprise read and write commands.

Claim 54 (New) The controller of claim 1, further comprising a cache manager for communicating with a cache memory.

Claim 55 (New) The controller of claim 54, wherein said cache manager determines whether data corresponding to said associated logical block address is stored in the cache memory before said command decode subsystem communicates said associated logical block address to said mapping controller, and if data corresponding to said logical block address is stored in the cache memory, said host command is processed using said cache memory and said command decode subsystem does not communicate said associated logical block address to said mapping controller.

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Claim 56 (New) An integrated input/output controller integrated into a single integrated circuit device, comprising:

a microcontroller subsystem for processing non data flow type host commands; and

a data flow subsystem for processing data flow type host commands, said data flow subsystem comprising,

a mapping controller for translating a logical block addresses of data flow type commands to peripheral block addresses;

a peripheral interface subsystem for accessing at least one peripheral;

a host interface subsystem comprising:

a host exchange controller for maintaining a host exchange table comprising a plurality of table entries, receiving a host command, adding a new table entry to said host exchange table corresponding to said host

command, each table entry being associated with a tag, and outputting the tag associated with the new table entry; and

a command decode controller for maintaining a command queue comprising a plurality of queue entries, receiving the tag associated with the new table entry, adding a new queue entry corresponding to said tag, and outputting a cache manager packet;

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a cache manager subsystem for managing a cache memory, wherein said cache manager subsystem:

receiving the cache manager packet, if data associated with said cache manager packet is stored in the cache memory;

forwarding read data from the cache to the host exchange controller if the host command is a read command;

accepting write data from the host exchange controller if the host command is a write command; and

if data associated with said cache manager packet is not stored in the cache memory, forwarding a logical block address associated with said cache manager packet to the mapping controller to receive an associated peripheral block address, said peripheral interface subsystem accessing at least one peripheral using said associated peripheral block address.

Claim 57 (New) The controller of claim 56, wherein data flow host commands comprise read and write commands.

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Claim 58 (New) The controller of claim 56, wherein said mapping controller is capable of accepting a logical block address for a virtual volume which spans a plurality of peripherals and translating said logical block address to an associated peripheral block address.